"Express Mail" mailing label number:

EL989616983US

RECONFIGURABLE TERMINAL

Jerrell Hein

Field of the Invention

[1001] This application relates to communication with an electronic device and more particularly to dual use of a communication terminal.

Description of the Related Art

[1002] In the crystal oscillator (XO) and voltage controlled oscillator (VCXO) markets, standard low cost 4 or 6 pin XO and 6 pin VCXO packages having standard inputs/outputs (I/Os) are commonly used. In order to provide greater flexibility, some XO and VCXO devices include both an integrated circuit (IC) and a crystal (or surface acoustic wave (SAW) device), supplying a source frequency, in the package. In order to program and/or calibrate such XO or VCXO devices, some prior art approaches have used additional pins or contact points on the package to supply one or more programming parameters that determine the output frequency supplied by the XO or VCXO device. The use of extra package pins or contact points to provide programmability may require custom packages, which can result in additional package size, additional tooling and higher manufacturing costs. In addition, there may be a marketing disadvantage from using a non-standard package. Thus, for certain applications, additional package pins for programming may be undesirable. Other prior art techniques have utilized existing package pins for such programming.

[1003] In prior art devices, in order to program the output frequency, one or more parameter(s) are supplied to the XO or VCXO device, the output frequency is measured, and, if necessary, new parameters are supplied to adjust the output frequency. Such calibration can be time consuming. In addition, the parameter(s) appropriate for one crystal and semiconductor device pair may need to be adjusted for other crystal/semiconductor device pairs.

[1004] Rather than program through package pins, some prior art techniques use an open top package with additional connection points on the integrated circuit in order to calibrate the device prior to packaging. However, programming with an open lid on the package may not be desirable because after calibration with the open lid, the device characteristics can change after the lid is sealed, at least partially defeating the calibration efforts. If the device is not programmable at all, the inability to program a device means that the device lacks flexibility and calibration features.

[1005] Accordingly, it would be desirable to provide a flexible device for crystal oscillator (XO) and voltage controlled oscillator (VCXO) applications with improved programming and calibration capability.

SUMMARY

[1006] Accordingly, according to an embodiment of the invention, a device is provided for use in, e.g., XO and VCXO applications that utilizes a terminal that can function in a first mode as a serial communications port and in a second mode as an output enable terminal controlling, for example, the clock output(s). In the first mode, the output enable function is unavailable through the terminal. After the terminal is programmed to operate in the second mode, the terminal functions permanently in the second mode.

[1007] In one embodiment a method is provided that includes utilizing a terminal in a first mode of operation in which serial communications are received over the terminal and subsequently converting the terminal to a second mode of operation in response to a received command, in which the terminal functions as the input control for selectively enabling an output according to a value of terminal voltage.

[1008] In another embodiment, the invention provides a device that includes a terminal and control circuitry coupled to the terminal to permanently convert the terminal from a first mode of operation in which serial communications are received over the terminal into a second mode of operation in which the terminal functions to selectively enable an output according to a voltage value on the terminal.

BRIEF DESCRIPTION OF THE DRAWINGS

[1009] The present invention may be better understood, and its numerous objects, features, and advantages made apparent to those skilled in the art by referencing the accompanying drawings.

[1010] Fig. 1 illustrates a device according to an embodiment of the present invention having an integrated circuit and a crystal packaged in a standard six pin VCXO ceramic package.

[1011] Fig. 2 illustrates a device according to an embodiment of the present invention having an integrated circuit and a crystal in a configuration in which they are packaged in a standard four pin XO ceramic package.

[1012] Fig. 3 illustrates an embodiment utilizing a multi-function output enable input/output terminal that provides a serial communication terminal and an input terminal for receiving a configuration clock.

[1013] Fig. 4 illustrates an embodiment in which P1 and P2 I/O terminals provide a serial communication terminal for programming and for receiving a configuration clock.

[1014] Fig. 5 illustrates exemplary read and write formats utilized for communicating over the serial port.

[1015] Fig. 6 illustrates exemplary use of Manchester encoding for data supplied over the serial port.

[1016] Fig. 7 illustrates exemplary use of a calibration clock over the serial port.

[1017] Fig. 8 illustrates an exemplary embodiment of the digitally controlled oscillator utilized in Figs. 3 and 4.

[1018] The use of the same reference symbols in different drawings indicates similar or identical items.

DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[1019] Referring to Fig. 1, a high level block diagram of an embodiment of the invention includes an integrated circuit 10, described further herein, coupled to a crystal 11. Both the integrated circuit 10 and the crystal 11 are packaged in a standard ceramic package 15 that is typically utilized for packaging a voltage controlled crystal oscillator (VCXO). Typical packages sizes are 5X7 mm and 9X14 mm. In one embodiment the crystal used is a third overtone 116.64 MHz crystal. Note that another resonating device such as a surface acoustic wave (SAW) device may be utilized in place of crystal 11. The package 15 includes standard input/output signals including a voltage control input 17, a power and ground input, 19 and 21 respectively, clock out plus and minus 23 and an output enable pin and terminal 27.

[1020] Referring to Fig. 2, a four pin XO package implementation is illustrated in which the control voltage input 17 is not utilized and the output clock 29 is single ended. In a six pin XO package configuration, the control voltage input on the package is not connected when the package 15 is mounted to a board.

[1021] Note that the terms "pin" and "terminal" as used herein are intended to refer to any kind of electrical connection provided on a package or integrated circuit such as a pin on a package or a contact pad on an integrated circuit. The term input/output (I/O) terminal (or pin) is intended to mean either a terminal that functions as an input, an output or both.

[1022] Table 1 shows industry standard input/output (I/O) for four pin and six pin XOs and six pin VCXOs. As can be seen from these Table 1, there is one common static input in all of the packages – the Output Enable/Disable (OE) pin.

[1023] TABLE 1

I/O	4 PIN X0	6 PIN XO	6 PINVCXO
1	Power	Power	Power
2	Ground	Ground	Ground
3	Clock Out	Clock Out +	Clock Out +
4	Output Enable/Disable	Clock Out -	Clock Out -

5		No Connection	Control Voltage
6		Output Enable/Disable	Output Enable/Disable

[1024] In order to provide a more flexible clock device, according to an embodiment of the present invention, the OE pin 27 is multi-functional. That is, in one embodiment, the OE terminal functions as a normal enable signal causing the output clock(s) to be either supplied or not according to the voltage level on the OE terminal. In addition, according to an embodiment of the present invention, the OE terminal 27 is also used for programming and calibrating the device 10. In order to program the integrated circuit device, the OE terminal 27 is used to communicate serial data to and from the integrated circuit 10. Thus, in addition to normal enable/disable functionality, in one embodiment of the invention, the OE pin 27 serves as a serial port for access to storage locations internal to integrated circuit 10, thus providing programmability. In an embodiment, the OE pin is bi-directional, implemented as an open drain with a weak pull-up. In some embodiments, the serial communication may be unidirectional into integrated circuit 10.

[1025] In addition, OE terminal 27 can function as a calibration input used to internally generate calibration correction factors using an internal PLL. The calibration input receives a calibration clock providing a frequency reference for calibration. The calibration clock feature is useful, e.g., so that the device can lock its output clock to the calibration clock using an internal PLL, and correction factors used to lock the PLL to the calibration clock can be stored for absolute output frequency and/or frequency versus temperature, as described further below.

[1026] Adapting the OE terminal to be multi-functional provides both programmability and calibration capability, and because a standard input terminal is utilized for the functions, no special packaging is required, resulting in low cost for the additional functionality. Significantly, the functions can be performed after the device is packaged and sealed. In addition, low frequency test equipment can be used to provide programming and calibration of the devices in a sealed package without any additional package pins.

[1027] Referring to Fig. 3, a block diagram illustrates an embodiment of integrated circuit 10 utilized in a six pin VCXO package implementation. In the illustrated embodiment, implementing the multi-functional OE terminal 27 is accomplished as follows. The output enable signal supplied from an external source to OE terminal 27 is provided to control circuit 30, which may include a sampling circuit and a state machine. The control circuit 30 determines whether the received signal is a valid output enable signal, serial data communication, or a calibration clock. If the signal on OE terminal 27 is determined to be a valid output enable signal, then the signal value on OE pin 27 is utilized to generate an internal output enable control signal 31, which in turn enables (or disables) output drivers 33 that supply the differential clock outputs CLKOUT+ and CLKOUT-.

[1028] Control circuit 30 determines whether the signal present on I/O terminal 27 is a valid output enable signal, serial data, or a calibration clock as follows. An internal oscillator clock asynchronously oversamples the OE I/O terminal. Any static value (all samples having the same value) that persists more that a predetermined time period, t_{STATIC}, is interpreted as a change to or as a valid enable/disable signal and the output clocks are selectively enabled or disabled based on that static value. The time period t_{STATIC} may be programmable. The sampling circuit functions as a deglitching circuit ensuring that short term changes on I/O terminal 27 do not cause changes to the enable/disable control of the output clock terminal(s).

[1029] In order to provide bi-directional data communication via I/O terminal 27, a bi-directional serial data format is utilized that includes guaranteed transitions at less than t_{STATIC} intervals. In one embodiment, the serial data format includes an indication of read or write, the register or other internal address, and direction (either data input or output). Because transitions of the serial communication are guaranteed at less than t_{STATIC} intervals, activity on the OE I/O terminal for serial data I/O will not interfere with the normal enable/disable functionality. In addition , a serial data format is selected that is sufficiently complex, e.g., with appropriate error detection capability, to preclude the possibility that a glitch at the OE terminal during normal operation would be inadvertently interpreted as a serial port command.

[1030] In order to distinguish between calibration clocks and serial data, a serial data command is utilized that indicates to the device that the calibration clock will be

applied next. That command enables the calibration PLL. After this command, the user supplies the low frequency clock to the OE terminal. The frequency of the calibration clock may be low even though the output frequencies are high due to the use of the divider 37 in the feedback path from the oscillator 39. Note however, that the frequency of the calibration clock should be high enough to provide transitions at less than t_{STATIC} intervals so as not to interfere with the normal enable/disable operation.

[1031] The device illustrated in Fig. 3 can function as a voltage-controlled crystal/ SAW oscillator (VCXO/VCSO) or as a fixed-frequency clock source (XO/SO). A register bit setting may be used to select between the modes of operation. In voltage-controlled oscillator operational mode the VC analog voltage input port 43 (see Fig. 1) and the on-chip analog to digital converter (ADC) 45 is used to convert VC into the digital frequency control word for the DCO. When operating as a fixed-frequency clock source (XO/SO), the ADC 45 is powered down and its output is fixed to its mid-scale value.

[1032] Referring to Fig. 4, in another embodiment the option is provided for using one of two dedicated I/Os on the integrated circuit device. The P1 port 81 is a dedicated I/O that functions as a bidirectional serial port for register data reads and writes, and as a calibration clock input, similar to the function of the OE pin used for programming and calibration described above but without any OE pin functionality. The P2 port 82 is also a dedicated I/O with the same serial bus and calibration clock functionality as P1; however, once programming is completed, P2 can be converted from a dedicated serial port I/O to an input control for the output enable function. Until the dedicated I/O functionality is disabled on P2, there is no output enable pin functionality provided by P2. At the initiation of manufacture test, before the on-chip non-volatile memory (NVM) has been written, either P1 and P2 are able to receive serial bus and calibration clock signals as dedicated I/Os (both should not be used at the same time). At the completion of the manufacture test programming of the various programmable registers, the user may write the programmable register values into non-volatile memory. P2 can then be programmed to function as an output enable control input causing its dedicated programmable I/O functionality to be permanently disabled. That may be accomplished by writing a keyword byte to a

programmable register (activate output enable register) to turn on the output enable functionality of the P2 pin and terminate the dedicated serial I/O functionality of the P2 I/O. That may be accomplished using logic gates enabling one function and disabling the other function according to the active output enable register value. P1 always is available to function as a serial and calibration clock port.

[1033] Writing the activate output enable register may cause the value to be written into the non-volatile memory (NVM). Alternatively, a specific command may cause the value in the activate output enable register (and other volatile storage) to be written into the NVM. Once the activate output enable register byte has been written into the non-volatile memory (NVM) with the appropriate keyword byte, the P2 I/O functions as the output enable input which controls the state of the clock output buffer. If the NVM is one-time programmable, the change is permanent. On power up or reset, the value in the NVM is loaded into the register to control the function of P2. The active polarity of the P2 I/O when it has been programmed to function as an output enable pin may be controlled by programmable register bits. In addition, register control of the output drivers may be provided. The state of the output driver when disabled (e.g. tristate, hold logic 0, or 1) may also be controlled by register control bits.

[1034] Similar to the OE pin described in relation to Fig. 3, an input deglitching circuit 83 guarantees that short term glitches or pulses on the P2 pin are ignored and do not affect the internal buffer disable control. The length of the deglitch interval, also referred to herein as (t_{STATIC}) may be programmable via programmable register bits, e.g., by programming the number of consecutive samples required for validation. In one embodiment, the number of samples varies between 1 and 1024. Similar to operation of output terminal 27 described above, all samples of the P2 input should have the same value for the entire duration of the deglitch interval before the state is validated and reflected at the internal buffer control. In one embodiment, the sample clock rate for the deglitch circuit is approximately 10 MHz ($f_{samp} = f_{osc}/512$).

[1035] The serial port is typically used during manufacture test to establish the desired device configuration in the on-chip non-volatile memory (NVM) 60. Serial port communications can begin following a power-on-reset of the device. An exemplary command format for the serial bus is shown in Fig. 5. Each transmission

consists of 3 eight bit bytes of data: the preamble byte 501, the instruction byte 503, and the address/data byte 505. One extra clock cycle 507 exists for the Read command in order to allow time for placing the transmit output of the test equipment hooked up to the device in high impedance before the first read bit is sent by the device. The serial port state machine, which may be part of deglitching circuit 83, returns to its initialized condition if any invalid input data is detected or if no activity occurs on the bus. That feature guarantees that the state machine can always be brought to a known condition before signaling begins. In one embodiment, all data sent from the test equipment (master) to the device (slave) is Manchester encoded with a symbol rate of approximately 10 kbps. The Manchester encoding creates guaranteed transitions in the data pattern that are used by the device to determine the master's transmission rate. In an embodiment, read data sent from the device to the test equipment is in a non-return to zero (NRZ) format, which maximizes the available sampling time for the test equipment master. The test equipment master can sample the read data using the same internal clock used to generate the transmit data.

[1036] TABLE 2

BYTE 1 Instruction	BYTE 2 Address/Data[7:0]	Comments
00000000	AAAAAAAA	Set Address
01000000	DDDDDDDD	Write
01100000	DDDDDDDD	Write and Increment Address
11000000	DDDDDDDD	Read
11100000	DDDDDDDD	Read and Increment Address
10100000	AAAAAAAA	Read Stored Address Value
10000000	XXXXXXXX	Reserved
00100000	XXXXXXXX	Reserved

[1037] Fig. 6 gives illustrates a Manchester encoded "0" and "1" and also shows the required preamble data pattern. Note that the preamble contains multiple Manchester code violations in order to increase its uniqueness and reduce the chances of false preamble detection.

[1038] Referring again to the embodiment illustrated in Fig. 4, the digitally-controlled oscillator (DCO) 39 is driven by a digital frequency control word M and produces a low jitter output clock. The control word M (50) supplied to the DCO 39 is generated by summing a reference frequency control word (RFREQ) with the VCO ADC 45 output (VCADC) and the temperature compensation value (DELMT) in

summer 49. The fixed frequency external crystal 11, SAW, or clock provides a low jitter reference needed to synthesize the output clock. In one embodiment frequency synthesis is done digitally, eliminating sensitive noise entry points. In one embodiment, the center frequency of the device is determined by the RFREQ DCO input and the HS_DIV and N1 output divider values.

[1039] In one embodiment different calibration approaches with increasing levels of accuracy may be utilized. For some applications, the inherent frequency accuracy and temperature stability of the on-chip crystal oscillator, SAW oscillator, or external reference clock may be sufficient. In this case, no calibration features are needed. A register bit may be used to disable the calibration correction features, in which case the temperature compensation (DELMT) value is forced to mid-scale.

[1040] In some applications it may be adequate to perform a one-time characterization of the device with the crystal or SAW type being used, deriving a set of nominal calibration correction factors from this characterization. Following the characterization, these calibration factors may be loaded into the memory of every device without individual calibration. This approach requires some time initially to generate the nominal calibration factors but does not require calibration of each device.

[1041] Alternatively, it is possible to individually calibrate each device, generating a unique set of calibration factors for each one. That approach addresses errors due to the performance parameters of each combination of the device and crystal or SAW. The highest level of error reduction is achieved at the cost of increased test time. Individual calibration is most feasible when each device and crystal or SAW is mounted and packaged together and then tested after packaging.

[1042] The method for frequency and temperature calibration of the DCO uses an external calibration clock applied at the serial port (the OE pin, P1 or P2). In calibration mode, a digital PLL is implemented around the DCO, locking the DCO output clock to an integer multiple of the low frequency input calibration clock. Once the calibration clock is applied, the device internally generates the required calibration correction factors to generate the desired output frequency.

[1043] With reference to Figs. 3 and 4, calibration according to an embodiment of the invention operates as follows. First the temperature compensation DELMT (delta M over temperature) should be turned off. That forces its contribution to summing node 49 to 0. If desired it may be enabled after the calibration is complete. If the device is being used as a VCO, VCO mode should be enabled and the analog input V_C 43 should be set to its mid-scale voltage during the calibration. That sets the analog to digital converter 45 at midrange. If the device is being used as a fixed frequency oscillator, VCO mode should be disabled to cause the output of the ADC 45 to be at midscale and thus not affect the output frequency. Next the calibration clock frequency range (N3 divider value) 35 should be selected. In one embodiment, there are two possible frequency ranges for the calibration clock. A register bit can be used to select the range from 1 to 2 MHz, (the divider value = 1). To select the range from 8 to 16 MHz, the input divider N3 is set to a divider value to 8. The choice of calibration clock frequency range is based on the availability of precision clock sources in the manufacturing test environment. Other embodiments may have different values for the divider block N3 or lack the divider block entirely.

[1044] The values for dividers 35 (N3), 37 (N2), high speed divider (HS_DIV) 38 (Fig. 4) and 61 (N1) should be selected along with the calibration clock frequency. The equation relating the calibration clock frequency to the output frequency is as follows for one embodiment of the invention.:

$f_{OUT} = f_{CALCK} \times N2/(HS\_DIV \times N1)$ (for N3=1), or

$f_{OUT} = f_{CALCK} \times N2/(8 \times HS\_DIV \times N1)$ (for N3=8),

where HS_DIV = [4, 5, 6, 7, 9, 11], $1 \leq N1 \leq 2^7$ and N2 = 256, 512, 1024

Other embodiments may provide other divider values, additional or fewer dividers and thus have different equations for determining the output frequency.

[1045] In some embodiments, the calibration loop bandwidth is also selectable. In one embodiment two choices for calibration loop bandwidth are available, which are selected according to a register bit. The wider bandwidth provides faster settling time, but allows more of the calibration clock phase noise to affect the absolute frequency accuracy when the DPLL is frozen. The lower bandwidth has slower settling, but less variation in the absolute frequency value when the DPLL is frozen.

The optimal choice is a function of the calibration clock jitter and the absolute frequency accuracy requirement for the application.

[1046] Referring to Fig. 7, the control circuit 30 then receives a command setting the calibration clock on (CCK_ON) register bit to one through a serial port register write, indicating that a calibration clock is to be supplied over the serial port (input/output terminal 27, P1, or P2). Subsequently, the calibration clock can be supplied as an input frequency reference for the calibration PLL. Fig. 7 illustrates a command sequence including a preamble, write command and data followed by application of the calibration clock. In response to the write command, the control state machine selects multiplexer input A from the digital phase detector and loop filter 51, which forms a phase-locked loop with DCO 39 in this configuration. The calibration clock (CALCK) is supplied via node 53 to the divider circuit 35. The digital phase detector and loop filter 51 detects the phase/frequency difference between the calibration clock and the output of the DCO 39 and provides a correction signal 58 to summer 49 through multiplexer 47 to adjust the control signal M supplied to the DCO 39 to reflect that difference. The calibration clock is applied for sufficient amount of time to allow the PLL to settle and establishing the correction factors needed to lock the DCO 39 output clock to an integer multiple of the low frequency input calibration clock. In other embodiments the DCO may lock to a fractional multiple (e.g., a ratio or integers) of the calibration clock according to the dividers utilized. Note that because of the divider 37 in the feedback path of the PLL, the calibration clock can be a low frequency signal even for those devices with high speed output clocks. Note that control operations during calibration, e.g., to select the multiplexer input and store the value of M, may be controlled via commands sent to serial port, the result of internal control generated by, e.g., a state machine in control circuit 30, or both.

[1047] Once the PLL is locked and settled the calibration clock is stopped as shown in Fig. 7. That causes the internal state of the device to be stored and the CCK_ON bit is automatically reset to zero. The cessation of the clock is detected by the control circuit 30 causing it to freeze the correction values internally. If the delay required to detect the cessation of the clock allows the PLL to be disturbed before the correction values are stored, a history of the correction values can be kept on-chip and

the correction values that existed before the actual clock cessation can be kept. The correction values that are stored may be the correction factor generated by the phase detector and loop filter 51 or the value of M when the PLL is locked to the calibration clock (essentially the same as the correction factor but after the summing node 49). To avoid any inaccuracies in the frozen register values due to the loss of clock detection delay, a running history of the values is kept and the values that existed immediately before the loss of clock are stored when the PLL is frozen. The running history may be stored in registers in the control circuit 30. The correction value(s), along with appropriate divider values, can be stored in the non-volatile memory 60, which may, e.g., be implemented as an EPROM, EEPROM, or any other suitable non-volatile memory. The correction value is used to generate the control value supplied to the DCO 39 by supplying the correction value to summing node 49 during normal operation.

[1048] In one embodiment a lock detection mechanism is included for the calibration PLL. A lock detect bit (LOCK) is the result of an analysis of the PLL phase detector output. A retriggerable one-shot is set each time the phase detector output indicates a full-scale condition (phase cycle slip). The retrigger time of the one-shot may be programmable via a register bit. Therefore, if no cycle slip has occurred for the retrigger time, the internal lock detection indicator bit (LOCK) is set to one, indicating that the PLL is in lock. The internal lock detection indicator bit (LOCK) can be queried to verify that the PLL achieved lock during the time the calibration clock was active.

[1049] Once the calibration clock has ceased for a sufficient amount of time defined by a predetermined time period, the internal over sampling state machine returns to its reset or initialization state, waiting for further activity on OE, P1 or P2, and ready to receive additional commands. This timeout feature prevents lockup of the state machine, guaranteeing a known starting condition for the user.

[1050] Note that the serial communication capability available through input/output terminal 27 also allows a user to program a fixed control value to set oscillator 39 to a specific output frequency by writing to frequency tune storage location 65 (referred to as RFREQ in Fig. 4), supplying that value to multiplexer 47 and selecting the B input of multiplexer 47 to be supplied to summing node 49.

Additionally, the divider ratios in any or all of divider blocks 35, 37, 38 and 61 may be written and/or read via the serial port provided by input/output terminal.

[1051] Note that calibration can also be performed without a calibration clock input. However, that requires multiple serial data writes to the device to set the correction factor supplied, e.g., through summing node 49 so that while the control voltage Vc is centered, the clock out signal matches an external calibration clock. By instead using a calibration clock supplied over the serial port, the device can itself find the desired correction value by locking its PLL to the calibration clock.

[1052] The on-chip nonvolatile memory (NVM) 60 provides for permanent storage of device configuration settings and calibration settings at manufacture. The NVM memory space includes bits for all of the settings necessary to fully configure the device. The volatile memory space includes duplicate bits for each NVM bit, plus additional bits that do not require nonvolatile storage. In one embodiment, the non-volatile memory is one time programmable. A primary (M1) and secondary (M2) NVM space are provided to allow the NVM settings to be written twice during the lifetime of the device. A status register may be used to indicate the current status of M1 and M2. Data is written from volatile memory, such as registers, into NVM using the STORE command. All volatile memory bits with duplicates in the NVM space are written with one command. The first time the STORE command is executed, the M1 NVM space is written. When the write is initiated, a status bit (M1_WR) is permanently set. Once the write is completed, STORE is reset to zero, a read of M1 is done, and the result is compared to the volatile memory settings. If there is a match, then the NVM write has been successful and the M1_CHK status bit is permanently set. The next time the STORE command is executed, the M2 NVM space will be written. After device powerup or reset, the NVM status bits are checked and the appropriate NVM memory space downloaded into the volatile memory. The appropriate NVM space may also be downloaded on command using the RECALL register bit. Once the download is complete, RECALL is reset automatically.

[1053] Upon power up, the device internally executes a power on-reset (POR) which resets the internal device logic, loads the various setting stored in the non-volatile memory into volatile memory (e.g. the various control registers), and places

the device output into high impedance. A register bit may also be used to initiate a reset.

[1054] As stated above, in one embodiment, the center frequency of the device is determined by the RFREQ DCO input and the HS_DIV and N1 output divider values. In one embodiment the device has the capability of storing four unique sets of RFREQ, HS_DIV, and N1 values representing four unique selectable output frequencies. There need not be a relationship between the four frequencies desired. This feature is useful in applications where a different output frequency is required depending on the system configuration. The FRQSEL[1:0] inputs 85 select which set of RFREQ, HS_DIV, and N1 values are used. If this feature is not desired, the FRQSEL[1:0] pins can be left floating, in which case default values are selected.

[1055] Note that the devices illustrated in Figs. 3 and 4 provide temperature compensation. That compensation is achieved by supplying the appropriate compensation value from non-volatile memory 60 based on the temperature detected by thermometer 67. Calibration for temperature compensation involves generating digital correction factors for various temperatures of interest.

[1056] In one embodiment temperature compensation values are determined as follows. First a reference temperature point is determined. The calibration at this temperature sets the RFREQ value to the DCO and all other temperature/frequency points are calculated with respect to this reference point. The reference temperature does not have to be the nominal ambient temperature of operation. To establish the reference temperature calibration point, a temperature calibration point register (TCP[2:0]) is set to 000, FRQSEL[1:0]=11 (if that feature is provided), and the device is brought to the desired reference temperature. The calibration clock is then applied through the P1 or P2 pin. When the clock is stopped, the M value corresponding to the frozen frequency and the temperature value are stored in the RFREQ_11 and RTEMP RAM registers, respectively. The stored values of M and the temperature are the values that existed immediately before the clock was stopped to avoid any glitches that might occur after the calibration clock is stopped.

[1057] To generate the calibration points across temperature, after establishing the reference temperature calibration point, TCP[2:0] is set to 001 to indicate the next

temperature calibration point is being established, and FRQSEL[1:0] is set to 11, and the device is brought to the desired temperature. The calibration clock is applied as described previously. When the clock is stopped, the frozen delta-frequency value (relative to RFREQ_11) is stored in the DELMT1 register. The frozen delta-frequency value = (M at the reference temperature) – (M at the next temperature calibration point). The associated temperature is stored in the TEMP1 register. For each additional temperature calibration point, the temperature calibration point register is incremented and the calibration clock is reapplied at the desired temperature, and the new frozen delta-frequency value is stored along with the corresponding temperature. The temperature and delta M values are subsequently stored in non-volatile memory. During operation the M value at the reference temperature is used when the thermometer 67 indicates the reference temperature and appropriate offsets (supplied as DELMT) are supplied according to the temperature detected by thermometer 67. In other embodiments, the value of M at the particular temperature is stored, rather than delta M, and that value is supplied for temperature compensation.

[1058] In one embodiment the device can store up to six calibration points (frequency and temperature pairs), including the reference point, to calibrate the device across temperature. In normal operation with the temperature compensation feature turned on, the device interpolates between the provided calibration points using a polynomial of order N-1, where N is the umber of calibration points to be used, which in one embodiment is programmable using register bits. For example, if values are written into RFREQ_11, DELMT1, DELMT2, and DELMT3 while DELMT4 and DELMT5 are not to be used, the user set N=4 so that a 3rd order polynomial interpolation is used.

[1059] As illustrated in Fig. 4, and described above a multi-frequency feature is available using the frequency select inputs FREQSEL[1:0]. If the multi-frequency feature is used, temperature calibration for the additional frequencies is achieved by holding the device at the reference temperature, setting FREQSEL[1:0]=10, and reapplying the calibration clock at the appropriate frequency. When the clock is stopped, the frozen frequency control value is stored in RFREQ_10. If a third and

fourth frequency are desired, repeat the above procedure with FRQSEL[1:0]=01 and 00, respectively.

[1060] Referring to Fig. 8, illustrated is an exemplary embodiment of the digitally controlled oscillator (DCO) 39. The crystal (or SAW) oscillator 11 (not shown in Fig. 8) provides one input 800 to the phase and frequency detector 801. Phase and frequency detector 801 generates an error term of the difference between the input 800 to PD 101 and the feedback from the VCO 805 supplied by the divide-by-N block 807. In the embodiment illustrated in Fig. 8, the DCO is a fractional-N frequency synthesizer in which the control value M (control value 50 in Fig. 4) is supplied to a delta sigma modulator 809, which in turn is used to adjust the value of N in the multi-modulus divide-by-N block 807 in the feedback loop of the DCO 39.

[1061] In order to additionally compensate for temperature variations, which affect the reference frequency supplied, e.g., by the XO, the delta M over T value (DELMT) value is supplied to summer 49 along with the reference frequency control value RFREQ. Thus, the control value generated at the reference temperature calibration point, along with an interpolated delta as described above, is supplied to summer 49 and utilized to generate the M value. Note that other temperature calibration algorithms besides the interpolation described above may be implemented in the algorithm block 111. That function, in the embodiment illustrated in Fig. 4, is performed by the control circuit 30. Thus, the temperature compensation is achieved by adjusting the feedback loop of the DCO 39 through the delta sigma modulator 109 coupled to adjust the divisor value in the divide block 107.

[1062] In one embodiment, the divide-by-N block 807 is formed by a series of dividers. Because the feedback frequency may be in the giga Hertz range, a prescalar is used to divide the feedback signal by, e.g., 4 or 5. Subsequent division stages, e.g., a plurality of divide by 4 and/or 5 stages further divide the feedback signal to an appropriate value according to the desired divider value.

[1063] Assume for example, that the value of M is 100. The temperature compensation value determined by the interpolation described above may cause the value of M with temperature compensation to be 100.5. The delta sigma modulator in one embodiment provides an output having 8 different integer levels from -3 to 4, to

represent the fractional portion, which values are combined with the integer portion (100) and mapped into the series of dividers in divide by N block 807. Thus, values ranging from 97 to 104 may be applied as divider values to the multi-modulus divide by N block 807. The use of the delta sigma modulator allows appropriate values to be used to average 100.5. Note that a value is generated by the divide by N block 807 at a rate of the XO (or other reference) clock frequency supplied on node 800. Note also that noise shaping may be used to place any noise generated in the feedback divider in a frequency band that may be subsequently filtered by a low pass filter in the loop filter 803.

[1064] Thus, various embodiments have been described for calibrating and utilizing a clock device. The description of the invention set forth herein is illustrative, and is not intended to limit the scope of the invention as set forth in the following claims. For example, while a PLL has been described other control loops, such as a frequency locked loop may be utilized to generate appropriate correction values to calibrate the oscillator. Other variations and modifications of the embodiments disclosed herein, may be made based on the description set forth herein, without departing from the scope and spirit of the invention as set forth in the following claims.